Stencil Nano-coatings – Do They Improve Repeatability and Uniformity in The Print Process?

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Abstract
Over the past few years, studies have shown that Nano-coatings can improve solder paste release and reduce underside cleaning in the print process. Many of these studies have focused on print volume and the improvement of transfer efficiency in small component printing.

This paper investigates whether Nano-coated stencils improve repeatability and uniformity in the print process for a range of components sizes. Repeatability and uniformity were defined as how tightly controlled print deposits were from print to print over time. Solder paste inspection (SPI) data was collected and analyzed for the following component types: 01005 up to 1206 Imperial chip components; 0.5mm pitch micro BGA components; 0.4mm pitch up to 1.25mm pitch QFP components and 0.4mm pitch up to 0.6mm pitch QFN components.

Introduction
Nano-coatings for Surface Mount Technology (SMT) stencils have improved over the past several years. These coatings are hydrophobic and oleophobic and repel water, oil and solder paste flux. Some benefits of using these coatings are improved transfer efficiency, reduced need (or frequency) of underside cleaning, and reduced bridging after print. Nano-coatings have also been shown to create a more defined paste brick and print definition [1]. The primary focus of nano-coating research in relation to SMT stencil printing has been on paste release or transfer efficiency and reduced underside cleaning [2]. One area not explored, however, is the impact of stencil coatings on printed solder paste print area and print height.

Currently, there are two types of Nano-coatings being used on SMT stencils. The first is the Self Assembled Monolayer (SAM) coating. SAM coatings are manually applied to the underside or board side of the stencil where the foil contacts the Printed Circuit Board (PCB). The thickness of these coatings are typically 2-4 nanometers (Figure 1) and they are invisible. Validation of SAM coating presence is accomplished by testing surface energy. This is typically done with markers or surface energy inks (Figure 2). SAM coatings eventually wear off and can be reapplied. The primary benefits of these coatings are reduced underside cleaning and reduced bridging [3].

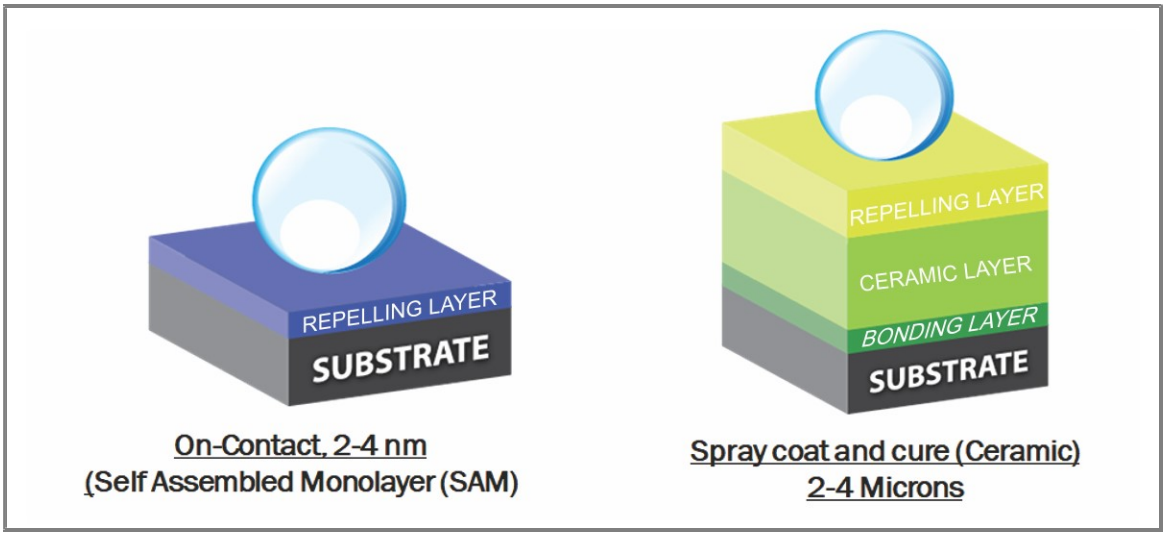

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Figure 1 – SAM and Ceramic Coating Image

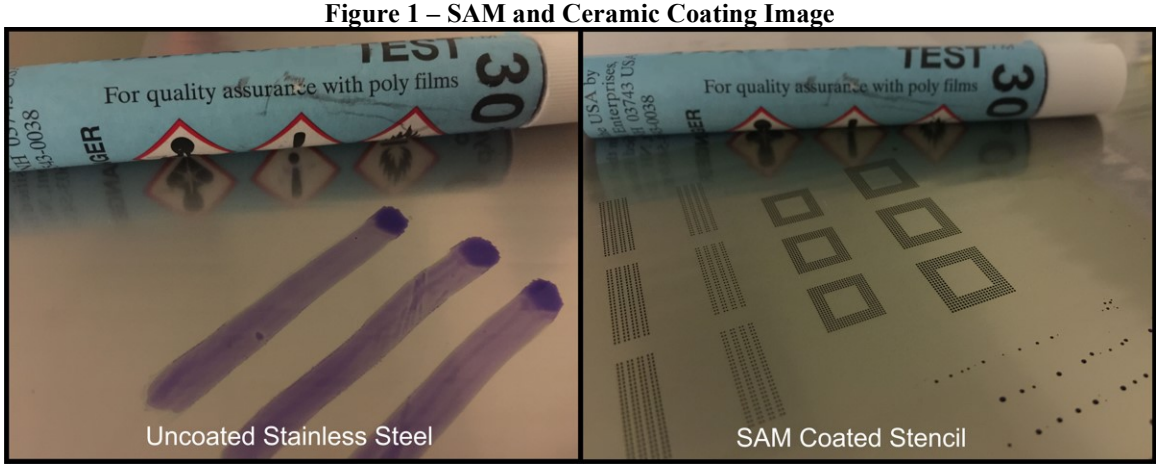

Figure 2 – SAM Coating Test

Ceramic Nano-coatings are applied using precision spray equipment capable of producing extremely small droplets sizes and are applied to the board side of the stencil and in the aperture walls. The thickness of these ceramic coatings is 2-4 microns (Figure 1) and they contain a colored dye. Some coatings also contain a UV indicator which allow coating presence to be detected with a UV microscope. After the ceramic coating is applied, a controlled curing process is used creating a hard, durable surface. The primary benefits of Ceramic Nano-coatings for SMT stencils are improved transfer efficiency, especially for small area ratio printing, reduction in underside cleaning frequency and reduced bridging after print.

In many board designs today, a range of component sizes are placed on the same PCB and process repeatability and uniformity are crucial to successful assembly. It has been stated that using nano-coating technologies allows larger foil thickness to be utilized for larger components while allowing successful area ratio printing down to 0.5 or even lower [3]. Transfer efficiency must be optimized for small area ratio aperture printing but, in addition, overall paste deposit area and height must be controlled to maximize overall process control. The purpose of this paper is to establish the effect of both types of Nano-coatings on volume, height and area across a spectrum of components.

Experimental Methodology

A test vehicle was created with a wide array of components including chip components from 01005 thru 1206, 0.4mm pitch CSP and 0.5mm pitch micro BGA, 0.4mm pitch QFN, 0.5mm pitch QFN, 0.65mm pitch QFN and 0.4mm pitch QFP thru 1.27mm pitch QFP were used. The test vehicle is shown below (Figure 3).

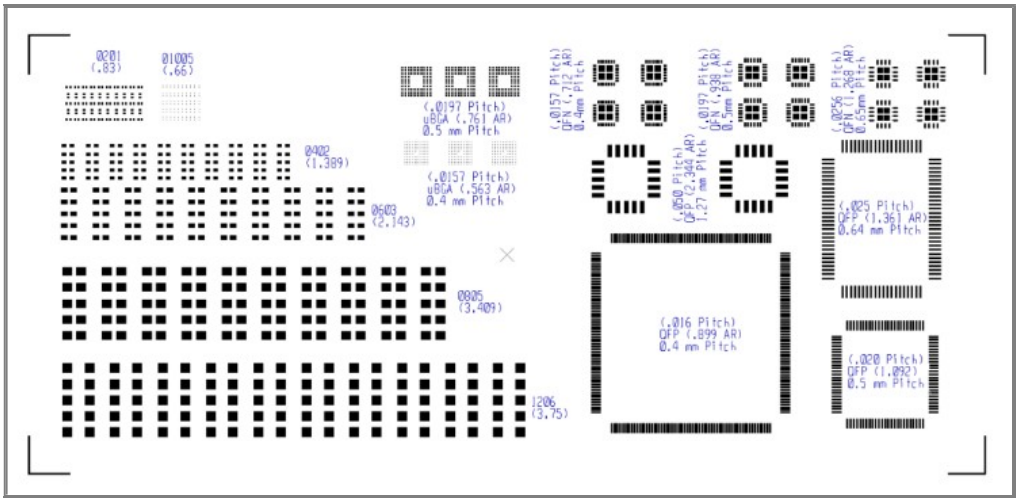

Figure 3 - Test Vehicle

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The test vehicle pattern was laser cut into each stencil and three stencils were cut on the same laser on the same day. Four-mil thick foil with a grain size of 6-10 microns was used for all three stencils. One stencil was not coated, one stencil was coated with a SAM coating after cutting and one stencil was coated with a ceramic nano-coating after cutting. (Figure 4).

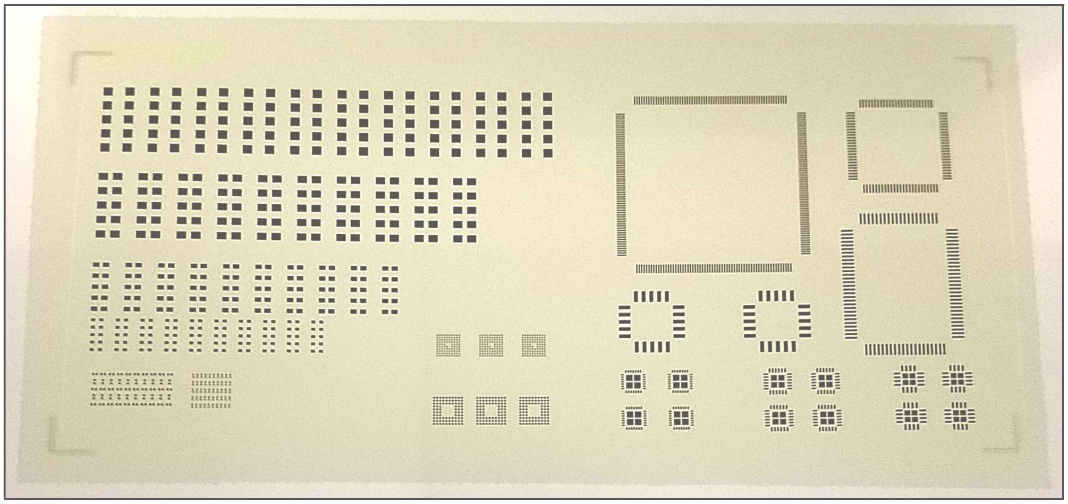

Figure 4 - Test Stencil with Ceramic Nano-Coating

A fifty-print study was run for each stencil using a no clean SAC305, Type 4 solder paste. The stencils were printed on bare copper clad material 0.062" (1.57mm) thick. Underside wiping was done after every two prints and a wet, vacuum, vacuum cycle was used. Print parameters are show below (Table 1).

Table 1 - Solder Paste Printer Parameters

Parameter	Value
Squeegee Length	300 mm
Squeegee Pressure	5 Kg
Squeegee Speed	30 mm/sec
Squeegee Angle	60 degrees
Separation Speed	3.0 mm/sec
Cleaning Solvent	IPA
Cleaning Cycle	2 Prints (W, V, V)
Solder Paste	NC SAC305 T4

Solder paste volume, area and height were measured using a 3D solder paste inspection system (SPI). The first, tenth, twentieth, thirtieth, fortieth and fiftieth boards were measured for a total of 6 boards measured with each stencil. The print data was analyzed using statistical analysis software and the results follow.

Results

Solder Paste Transfer Efficiency

When comparing transfer efficiency (TE) of the three stencils in relationship to only chip components (Figure 5), one can see that as the components get smaller, the Ceramic Nano-coating improves TE while the SAM coating decreases TE when compared to uncoated stencils. For the smaller chip components, the SAM coating decreased

TE while the Ceramic coating increased TE. As the chip components became larger, this difference in coating performance was reduced.

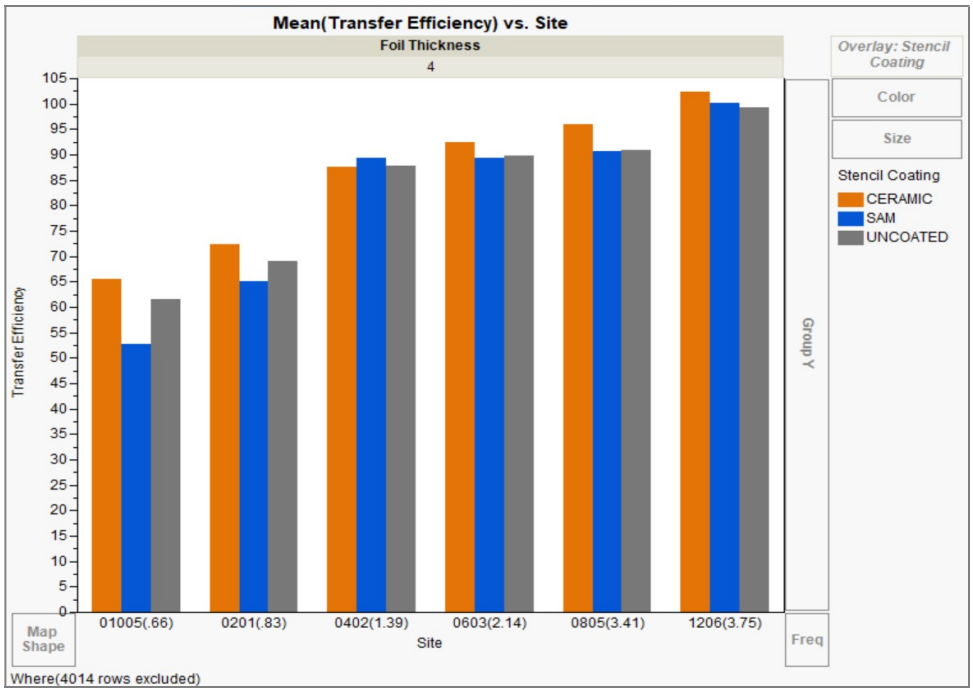

Figure 5 - Transfer Efficiency of Chip Components

When looking at the components with the smallest area ratios, 0.56-0.83, once again, the Ceramic coating improves TE while the SAM coating either reduces TE or has no effect (Figure 6).

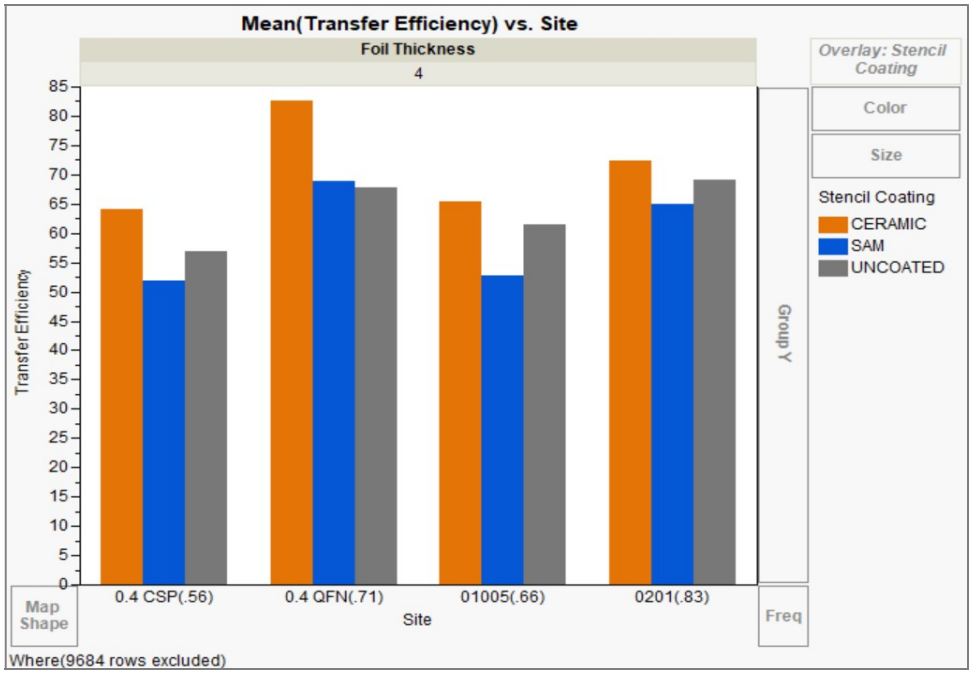

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Figure 6 - Transfer Efficiency of Smallest Area Ratio Components

Observing only the QFN and QFP components with area ratios ranging from 0.71 to 2.34 (Figure 7), improved TE is seen with the Ceramic coating up to 0.94 area ratio. Over 0.94 area ratio, both the Ceramic and SAM coatings show improvement over uncoated stencils for solder paste release.

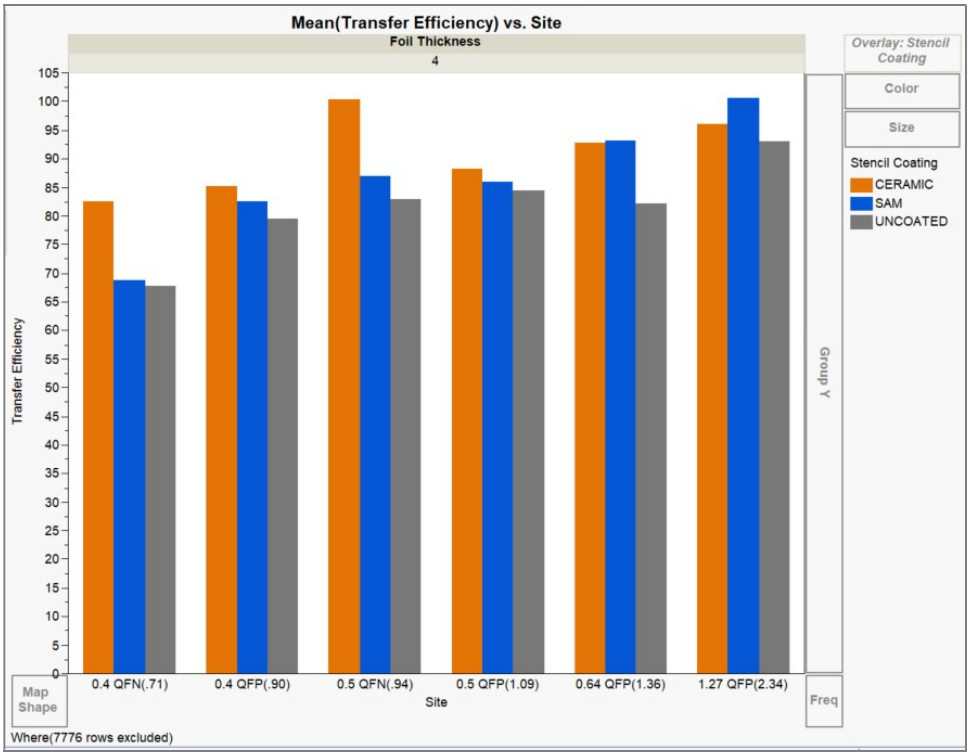

Figure 7 - Transfer Efficiency of QFN and QFP components

Finally, Tukey-Kramer HSD analysis is used to determine if there is a statistical difference in the TE performance of these two coatings in relation to an uncoated stencil. The results for the smallest area ratio components, 0.56-0.83 can be seen below (Figure 8). They indicate the Ceramic coating shows a statistically significant increase in TE versus an uncoated stencil and the SAM coating shows a statistically significant decrease in TE versus the uncoated stencil.

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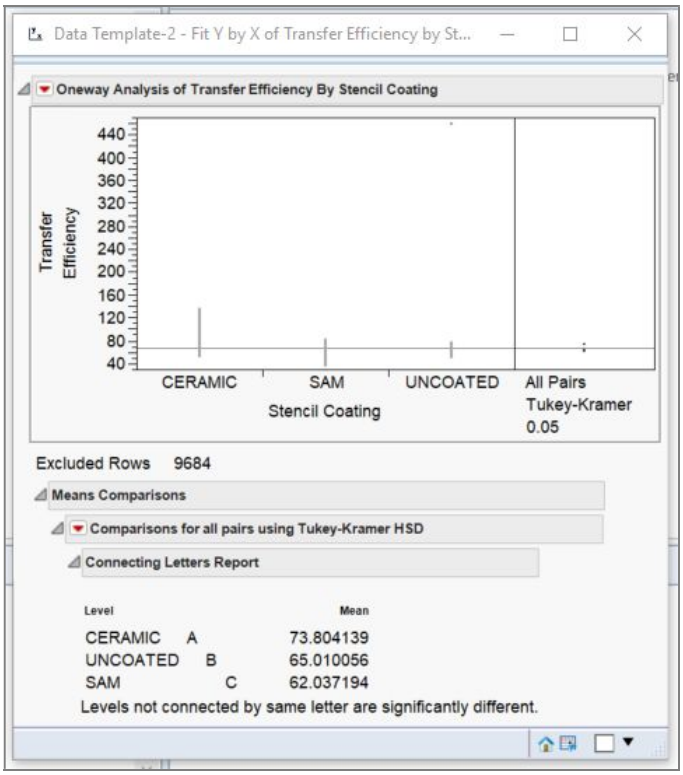

Figure 8 – Tukey-Kramer HSD on Transfer Efficiency of Small Area Ratio Components

Printed Solder Paste Height

During SPI inspection, paste print height was also collected. Since little work has been published on Nano-coatings and their effect on print height the intent was to determine if these two coatings influence paste deposit height.

In the chart below (Figure 9), printed height of chip components was measured. The stencil foil thickness was 4 mils and mean height measurements for all chip components was over 3 mils. The print height for 01005 and 0201 components was lower for the SAM coating than the Ceramic and uncoated stencil. This correlates to the print volume measurements in Figure 3 above showing the SAM coating volume for the 01005 and 0201 components is lower than both the ceramic and the uncoated stencil. In addition, the 0402 and larger chip component print heights for both the coated and uncoated stencils show little difference when compared to each other.

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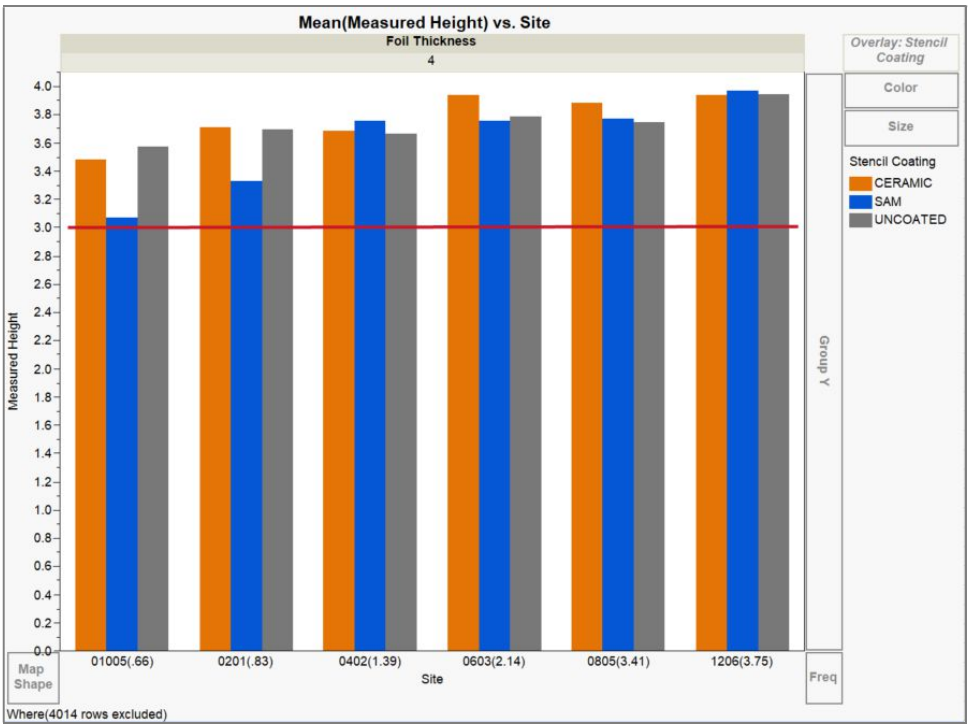

Figure 9 - Printed Height of Chip Components

Continuing to look at height measurement results, mean measured height results are shown for the 0.4mm pitch CSP, 0.4mm pitch QFN, 01005, and 0201 components in the chart below (Figure 10). Once again when comparing these height results to the volume measurement results in Figure 4 above, one can see they follow the same trend. For the 0.4mm pitch CSP, 01005 and 0201 components, printed heights are lower for the SAM coating than both the ceramic coated and uncoated stencils.

Overall, printed height for the ceramic coated stencil is slightly higher to the same as the uncoated stencil. Finally, when looking at the 0.4mm pitch CSP component, it can be seen that the reduced print height with the SAM coating falls below the 3-mil threshold. Based on these results SAM coatings are not preferred for small area ratio printing below 0.66 when 3-mil paste height is the lower limit for acceptance.

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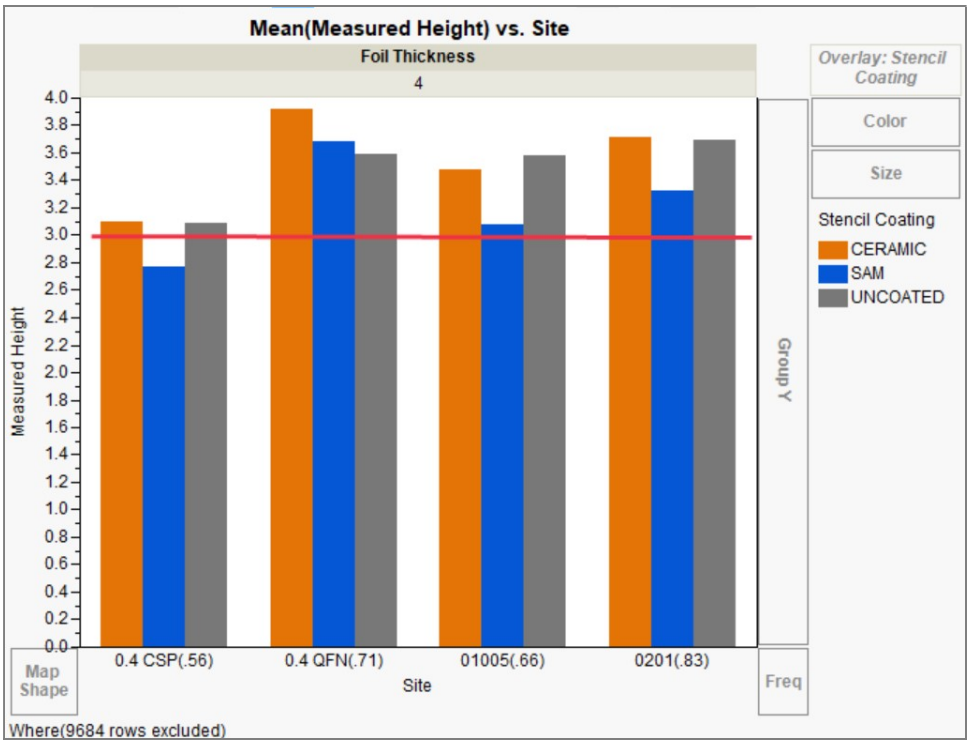

Figure 10 - Printed Height of Smallest Area Ratio Components

Finally, printed height measurements for QFN and QFP components are shown below (Figure 11). All of the heights are above the 3-mil threshold and the coatings only show a slight effect on height. Overall, the ceramic coating heights are higher or equal to the uncoated stencil and the SAM coated stencils exhibit slightly less improvement for these components with area ratios in the range of 0.71 to 2.34.

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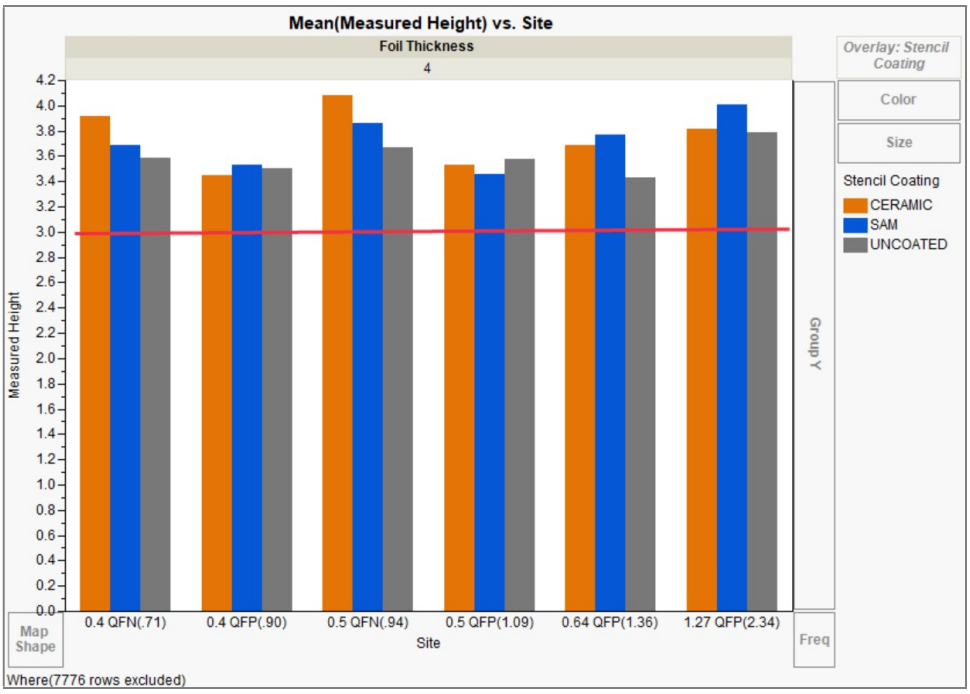

Figure 11 - Printed Height of QFN and QFP Components

The only components of concern when looking at paste print height data was the 0.4mm pitch CSP component with an area ratio of 0.56 and the 01005 component with an area ratio of 0.66. Print height mean data for both were below or close to the 3-mil limit. Tukey-Kramer HSD analysis can be used on the height data for these two components to determine if there is a statistically significant difference in the print height based on the coating type. If there is a statistically significant difference in these data sets based on coating, decisions about which coating to use when printing these components based on print deposit height may be made.

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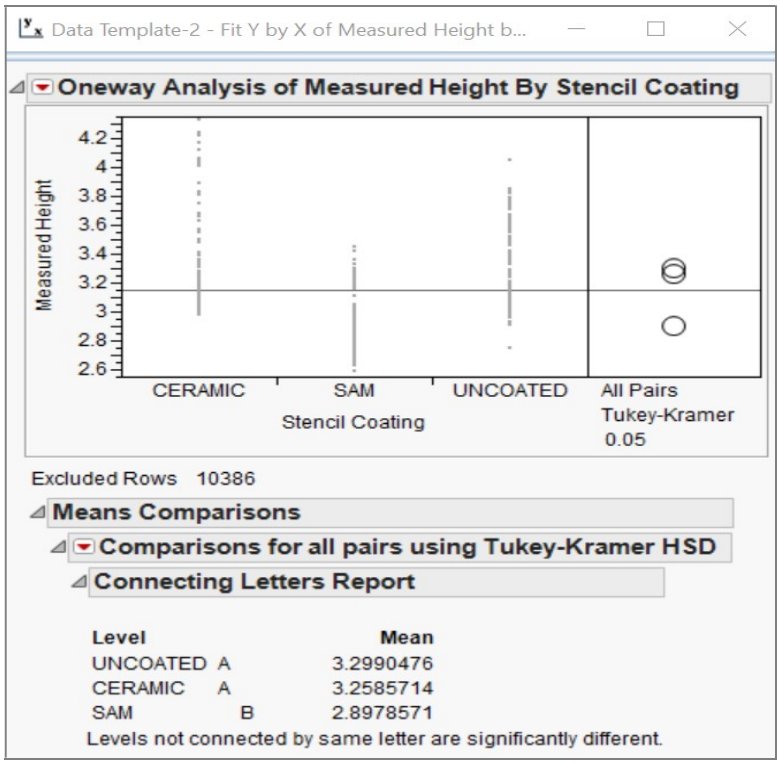

Figure 12 - Tukey-Kramer HSD Analysis on measured height of 0.4 mm pitch CSP and 01005 component

In the Tukey-Kramer HSD Analysis above (Figure 12) both the uncoated and Ceramic coated stencil print height data are significantly different than the SAM print height data. Mean print height data for the 0.4mm pitch CSP and 01005 components were above 3-mils for the uncoated and Ceramic coated stencils and under 3-mils for the SAM coated stencil. This indicates that SAM coatings may not be desirable for maintaining print heights above 3-mils for area ratios under 0.66 based on this data.

Printed Solder Paste Area

During SPI inspection, paste print area was also collected. Again, little data has been published on Nano-coatings and their effect on print area. The purpose of evaluating this print data was to determine if print area is influenced by nano-coatings.

In the chart below, the printed area percentage is shown for chip components ranging from 01005 through 1206 (Figure 13). It should be noted that printed areas for the 01005, 0.66 area ratio components were higher for the uncoated stencil than both the nano-coated stencils. The print areas for the larger components exhibit negligible differences with and without coatings. One theory for the higher print area on the 01005 components is the uncoated stencil is allowing paste to be deposited onto the underside of the stencil just around these apertures during the print process. As the squeegee fills and shears paste in the aperture, if the gasket is not perfect, paste will squeeze between the stencil and PCB. When the PCB releases, the paste will stick to the underside of the stencil and release to the PCB increasing the printed solder paste area. If the stencil has either the SAM or Ceramic coating, the paste will release to the PCB and not stick to the underside of the stencil. As a result, with the SAM and Ceramic coated stencils, the print from board to board will be more uniform. When the coating is not present, paste will not completely release from the bottom of the stencil and the gap between the bottom of the stencil will be larger on the next print. Larger area deposits will ultimately be made until under stencil wiping is completed.

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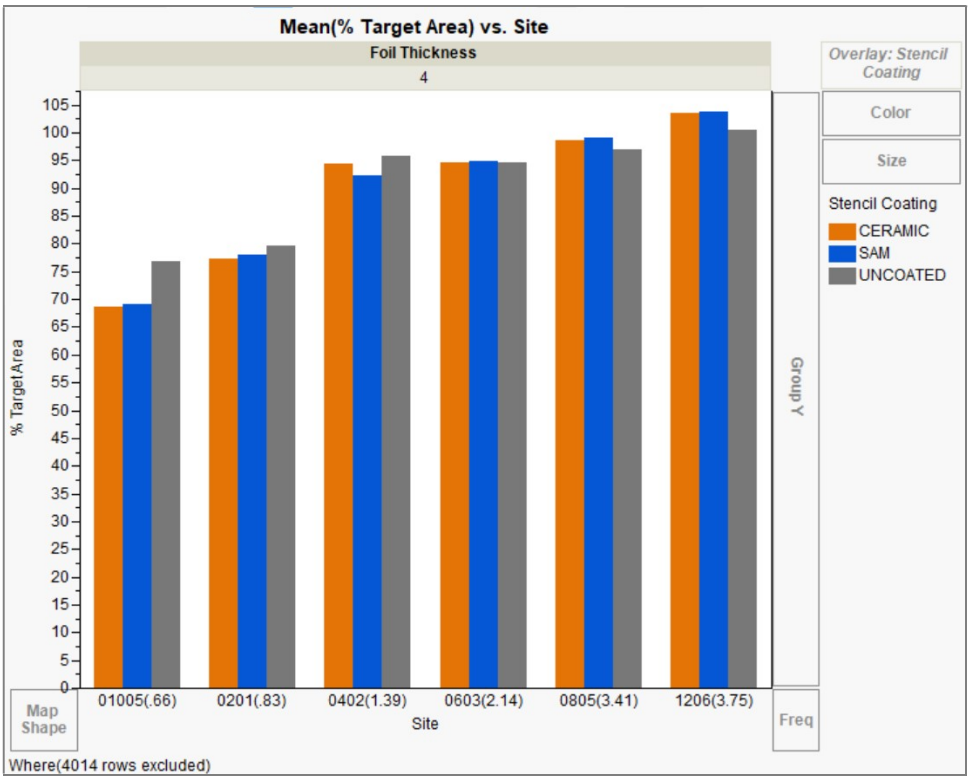

Figure 13 - Printed Area Percentage of Chip Components

The chart in Figure 14 shows mean target percentage of area measured in the SPI data for the smallest area ratio components. Since the 01005 components in this data was discussed in the previous chart, we will focus on the 0.4mm pitch CSP and the 0.4mm pitch QFN results. For these components, the Ceramic coating produced larger area percentage deposits than the SAM and uncoated stencils. A possible reason for this is paste released more completely from the Ceramic coated stencil than the uncoated and SAM coated stencils and created larger area percentage deposits on the small area ratio apertures.

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Figure 14 - Printed Area Percentage of Smallest Area Ratio Components

Finally, when looking at percent of target area for QFN and QFP components, the data in the chart below (Figure 15) also reflects that smaller area ratio apertures exhibit a larger percent area coverage when Ceramic nano-coatings are used. Again, the reasoning behind these results is paste is releasing more completely from the stencil aperture and creating a more defined brick. On the 0.5mm pitch QFPs and larger, slightly higher printed area coverage is seen with both the Ceramic and SAM coatings as compared to uncoated stencils.

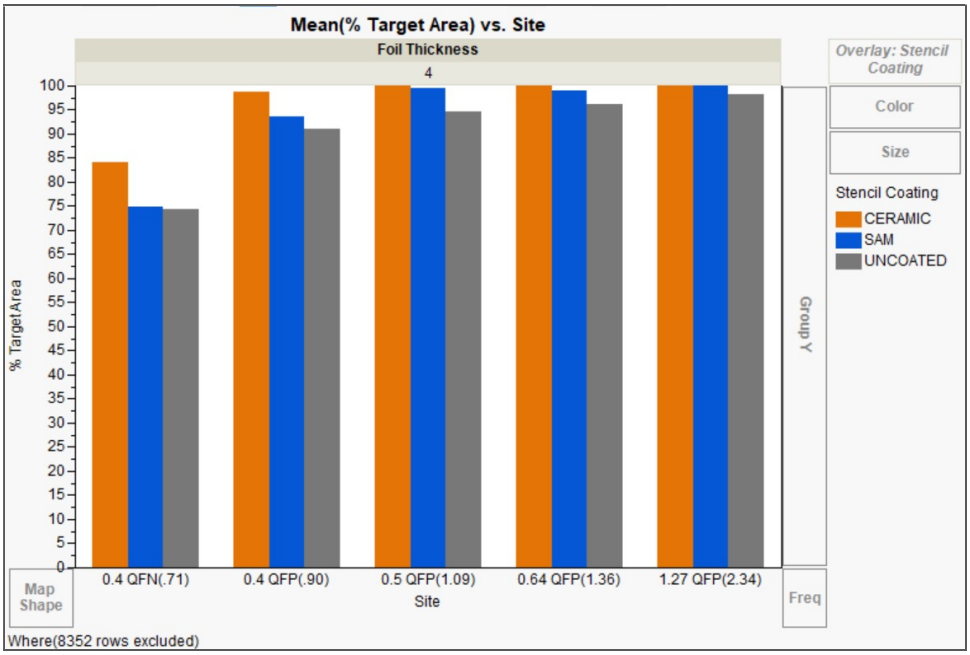

Figure 15 - Printed Area Percentage of QFN and QFP Components

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Conclusions

There are two types of nano-coatings used on SMT stencils today. The two types are self-assembled monolayer (SAM) nano-coatings and ceramic nano-coatings. Each type of coating has specific advantages and there is a significant cost difference in the two coatings. In this paper, the impact of these two types of coatings was compared against an uncoated stencil for print solder paste volume, height and area.

When comparing the coated stencil data results for print volume in relation to an uncoated stencil, the ceramic nano-coating improved print volume or transfer efficiency on almost all components tested. Small area ratio component apertures showed the largest improvement of transfer efficiency with ceramic nano-coatings. When evaluating self-assembled monolayer coatings for transfer efficiency on small area ratio apertures 0.66 and below, it was observed they decrease transfer efficiency. Although this reduction was minimal, for challenging assemblies where process optimization is critical, this coating may not be appropriate for area ratios of 0.66 or less. On larger area ratio components (above 0.66) adding the self-assembled monolayer coating, in most instances, did show a slight increase in transfer efficiency when compared to uncoated stencils.

Printed solder paste height data for each nano-coating tested was also collected. When the 0.4mm pitch CSP and 01005 printed height data was compared to uncoated stencil data for each coating, the ceramic nano-coating and uncoated stencil data were very similar. The self-assembled monolayer coating, however, showed a decrease in paste height lowering the print height for the 0.4mm pitch CSP component more than 1-mil from the foil thickness. For components larger than 01005, the self-assembled monolayer showed slight improvement over the uncoated stencil and the ceramic nano-coating showed the same or only slightly higher print height than the uncoated stencil.

Finally, solder paste print area was collected and analyzed. When looking at 01005 printed paste area, the uncoated stencil gave higher area data than the nano-coated stencils. This is believed to be caused by paste bleed under the stencil around the aperture during the print process. Since paste will not adhere to the underside of both the self-assembled monolayer and ceramic coating, the print area was the same for these coatings. Measured print area was higher for the ceramic nano-coating data versus the self-assembled monolayer and uncoated stencil for the 0.4mm pitch CSP, 0.4mm pitch QFN and 0.4mm pitch QFP component apertures. It is believed that this occurred because the ceramic nano-coatings release paste more fully creating a printed area close to nominal.

The overall results lead to the conclusion that ceramic nano-coatings should be used to optimize print characteristics when aperture area ratios fall below 0.66. For stencils with all aperture area ratios over 0.66 both ceramic and self-assembled monolayer nano-coatings are beneficial.

Future Work

Further investigation of both types of nano-coatings are ongoing. More work needs to be done evaluating coefficient of variation of each coating for volume, height and area as compared to uncoated stencils over time to further determine the effects of both nano-coatings.

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