Vapor Deposited Stencil Nano-Coatings-A New Break Thru or Just Another Coating?

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ABSTRACT
It is a proven fact that the addition of ceramic nano-coatings to SMT stencils improves transfer efficiency during the printing process. It has also been proven that these coatings also reduce the coefficient of variation more than other types of stencil nano-coatings currently available. Recently, CVD (Chemical Vapor Deposited) Nano-Coatings for SMT stencils have been introduced in North America. These coatings are thought to be more durable while still offering improved transfer efficiency. This paper explains the process of chemical vapor deposition and investigates its performance vs current nano-coatings being used. Coating thickness, chemical resistance, contact angle, and transfer efficiency will be looked at to determine if this new coating technology performs as well or better than current coatings in the market. The results will be summarized and presented to help those using or considering the use of nano-coatings to choose the correct coating for their application.
Key words: Nano-Coatings, SMT Stencil Nano-Coatings, Vapor Deposited SMT Stencil Coating, CVD SMT Stencil Nano-Coating, CVD, SMT Stencil Coating

INTRODUCTION
Component and board miniaturization continue to push the limits of printing solder pastes using laser cut stainless steel stencils. In addition, laser technology continues to improve along with the nano-coatings being applied to the stencils. The question we are still answering is how small technology will allow us to go. Currently, there are two types of Nano-coatings being used on SMT stencils. The first is the Self Assembled Monolayer (SAM) coating. SAM coatings are manually applied to the underside or board side of the stencil where the foil contacts the Printed Circuit Board (PCB). The thickness of these coatings is typically 2-4 nanometers (Figure 1) and they have no color. Validation of SAM coating presence is accomplished by testing surface energy. This is typically done with markers or surface energy inks. SAM coatings eventually wear off and must be reapplied. The primary benefits of these coatings are reduced underside cleaning and reduced bridging by reducing the ability of solder paste from sticking to the underside of the stencil.

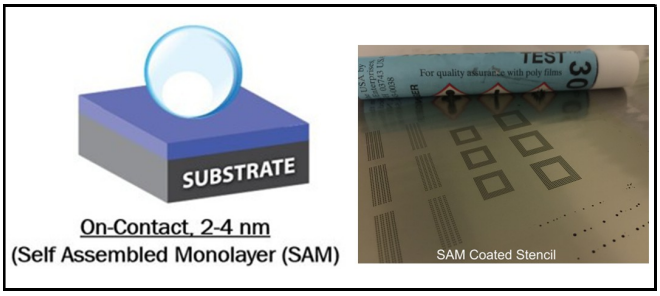

Figure 1. Self Assembled Monolayer Diagram

Ceramic Nano-coatings are applied using precision spray equipment capable of producing extremely small droplet sizes and are applied to the board side of the stencil and in the aperture walls. The thickness of these ceramic coatings is 2-4 microns (Figure 2), and they contain a colored dye. Some coatings also contain a UV indicator which allow coating presence on the aperture sidewalls to be detected with a UV microscope.

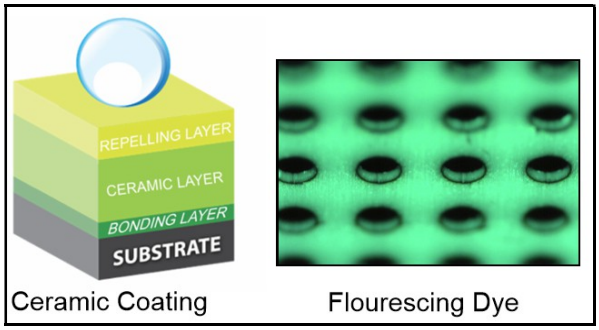

Figure 2. Ceramic Nano-Coating Diagram

After the ceramic coating is applied, a controlled curing process is used to create a hard, durable surface. The primary benefits of Ceramic Nano-coatings for SMT stencils are improved transfer efficiency, especially for small area ratio printing, reduction in underside cleaning frequency and reduced bridging after print. This is accomplished because the coating thickness fills the valleys of the laser cut sidewall of the aperture and creates a hydro/oleophobic surface that repels the solder paste flux which results in better transfer efficiency (Figure 3).

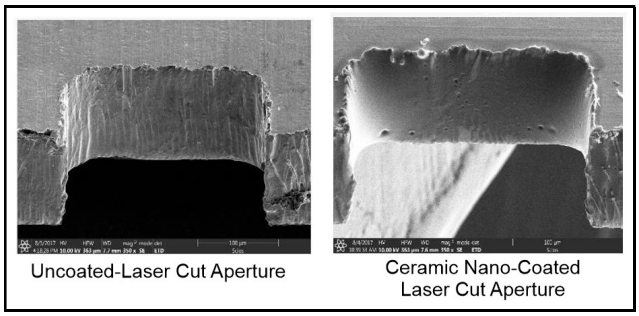

Figure 3. Uncoated vs Coated Ceramic Nano-Coating

Recently, a third type of stencil coating has been discussed in the industry. This coating is referred to as Chemical Vapor Deposition or CVD coating. This coating claims to offer hydrophobic and oleophobic properties resulting in similar benefits as current ceramic nano-coatings being used. This paper will examine the CVD process as applied to SMT Stencils and compare print results to current ceramic nano-coatings.

Wikipedia defines Chemical vapor deposition as "a vacuum deposition method used to produce high-quality, and high-performance, solid materials. The process is often used in the semiconductor industry to produce thin films. In typical CVD, the wafer is exposed to one or more volatile precursors, which react and/or decompose on the substrate surface to produce the desired deposit." (Figure 4) [1].

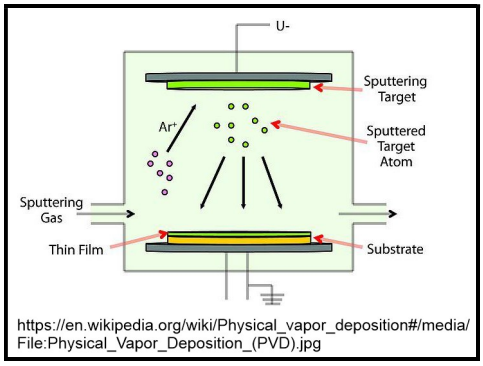

Figure 4. CVD Process Diagram

The process consists of "Targets" or "Precursors" comprised of proprietary materials that rotate in the chamber with the stencils to be coated. Once heat and vacuum are introduced, oxidation takes place, and these materials are vaporized and redeposited onto the stencil foil. These vapor deposited materials create layers of color and coatings to create a proprietary hydrophobic and oleophobic nano-coating.

METHODOLOGY

Materials

The circuit board used for this experimentation is shown below (Figure 5). This circuit board is made of FR4 material with an electroless nickel immersion gold (ENIG) surface finish.

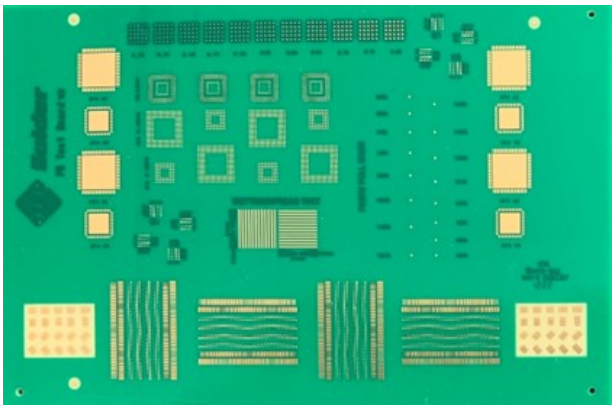

Figure 5. Test PCB for Print Testing

Four stencils were used for this experiment. All stencils used 5 mil Fine Grain (less than 5 micron grain stucture), stainless steel foil. All stencils were laser cut using the same program and mounted on 29x29 spacesaver frames. The only difference in each stencil was the stencil coating which is shown below (Table 1).

Table 1. Stencil Coatings Tested

	Foil Thickness	Coating
Stencil 1	5 MIL (.127mm)	None
Stencil 2	5 MIL (.127mm)	CVD1
Stencil 3	5 Mil (.127mm)	CVD2 (PP)
Stencil 4	5 MIL (.127mm)	NSG

Upon receiving the 4 stencils it was noticed that the CVD2 (PP) had a different appearance than the CVD1 coating. After further discussion and research, it was found that the CVD2 (PP) coating incorporated a plasma polishing process prior to applying the chemical vapor deposition process. This process is a "surface treatment resulting in very smooth, high-gloss surfaces with improved corrosion resistance" [2]. Both the surface of the stencil foil as well as the aperture sidewalls are polished with this process. The result of this subtractive process is a smoother sidewall prior to coating.

Stencil design matched the PCB test vehicle. The area of focus and testing for this experiment was on the mask defined arrays across the top of the PCB shown below (Figure 6). Specifically, aperture area ratios of 0.30 thru 0.65 were studied.

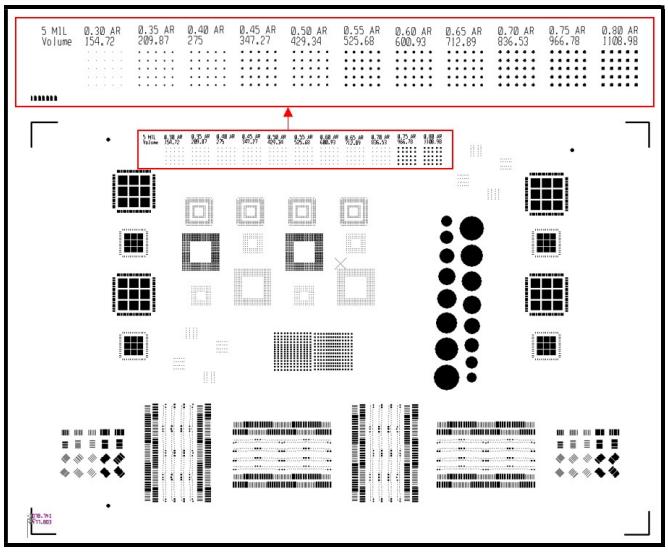

Figure 6. Stencil design of test PCB

The solder paste used in the print testing was a No Clean, SAC 305 Alloy, Type 4 solder paste.

ANALYSIS

Significant Difference Testing

Tukey Kramer honest significant difference (HSD) testing was done on the data sets to compare the data. Tukey Kramer HSD analysis determines whether multiple data sets are significantly different, or statistically similar. This test is similar to Student's t-test used to compare means. The output of the Tukey Kramer HSD test is a chart that shows the data sets, several data calculations, and reports (Figure 7).

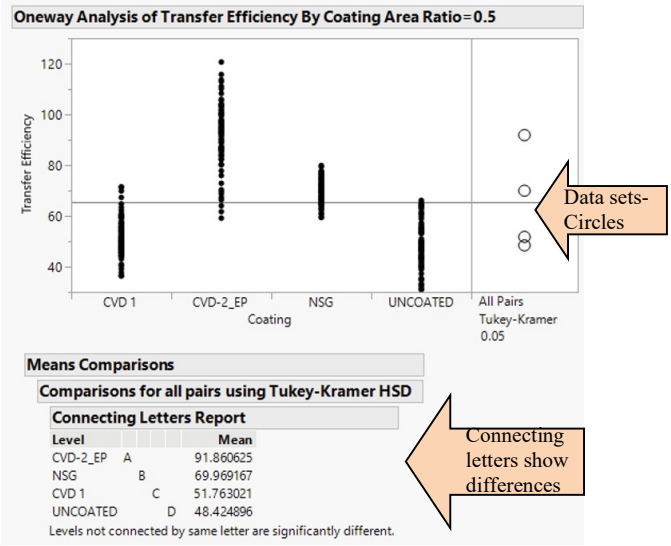

Figure 7. Explanation of Tukey Kramer HSD

The Tukey Kramer HSD analysis shows whether the data sets under comparison are significantly different. This analysis is used to draw general conclusions [3].

Process Capability and the Coefficient of Variation

The Coefficient of Variation (CV, CoV or CofV) is calculated as the standard deviation of a population divided by its means. Applied to solder paste deposits, CV represents the spread of the volume, height, area, or offset data. Because the average volumes of solder paste deposits vary based on many input variables, basic standard deviations should not be used to evaluate different distributions of data. Expressing the variation as a percent of the average normalizes it for better comparison [4].

As solder paste deposits become smaller, minimizing their variation becomes more critical:

- As passive devices get smaller, they are more prone to positional, rotational, or tombstone-type defects related to print quality.
- As integrated circuit packages get smaller and leadless, they are more prone to Head-in-Pillow, insufficient solder joints, voids and intermittent opens related to print quality.

Controlling the variation in print volumes limits the opportunities for defective solder joints and their associated rework or failure costs.

A widely accepted guideline for solder paste deposit CVs is:

- <10%: preferred
- 10-15%: acceptable
- >15%: unacceptable

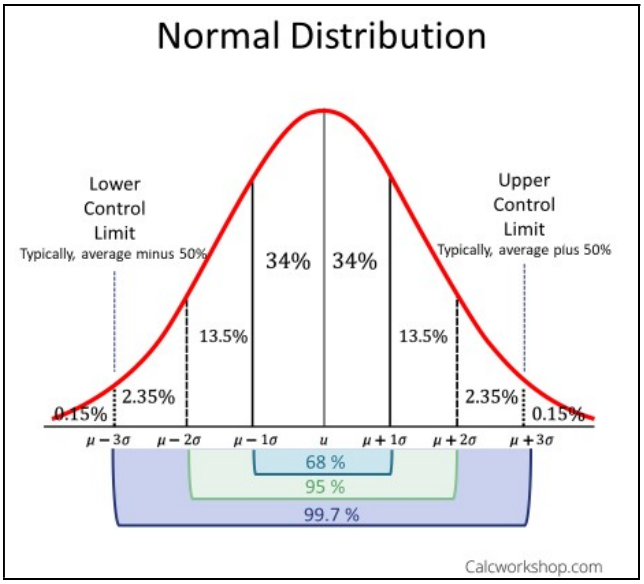

Figure 2. Normal Distribution as it relates to solder paste volume variation

These guidelines are based on principles of Statistical Process Control (SPC). Assuming a normal distribution of data as seen in Figure 2, 99.7% of the data should fall within +/- 3 standard deviations of the mean. If we apply a typical SPI control limit of +/- 50%:

- CVs of 10% will produce 99.7 % of deposits within +/- 30% of the target volume, leaving plenty of room for outliers or special causes of variation.
- CVs of 15% will produce 99.7% of deposits within +/- 45% of the target volume, leaving little room for variation.
- CVs of 16.7% or higher will produce deposits outside the control limits, indicating an out-of-control process.[2]

Transfer Efficiency

Transfer efficiency describes the volume of solder paste that is released from the stencil to the PCB as a ratio of the theoretical volume of solder paste in the stencil aperture.

Experimental Procedure

Initially, contact angle was measured for each of the stencil coatings. This was accomplished using a goniometer made for testing the contact angle of liquids placed on a surface. For this test, a precise droplet of deionized water was deposited on the coating, a camera in the goniometer captured an image of the droplet on the surface. The software then measured the angle of the bottom of the droplet to the surface. This is shown in the image below (Figure 8).

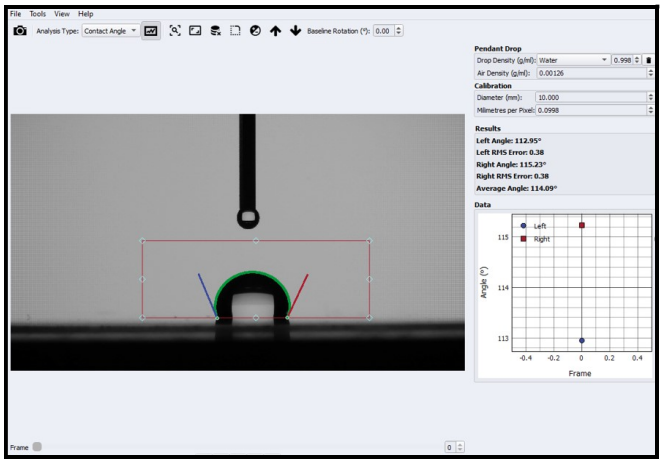

Figure 8. Goniometer Measurement using Di water

Looking at contact angle measurements, when the angle is higher, the surface is hydrophobic or repels the liquid (Table 2). When the contact angle is low, the surface is hydrophilic [4]. For solder paste stencils, the more hydrophobic the coating is, the better paste releases from the aperture sidewalls to the PCB.

Table 2. Hydrophobic vs Hydrophilic

Hydrophobic Surface		Hydrophilic Surface
High	**Contact Angle**	Low
Poor	**Adhesiveness**	Good
Poor	**Wettability**	Good
Low	**Surface Energy**	High

After the contact angle was measured, ten circuit boards were printed for each stencil variation. Standard parameters were used for printer settings. Once the boards were printed, solder paste volume, height and area were collected for each of the boards using solder paste inspection (SPI) and the data was analyzed for comparison. HSD Significant Difference and Coefficient of Variation (Cv) analysis was done to create conclusions.

RESULTS AND DISCUSSION

Contact Angle of Coating

Contact angle was measured on each of the stencils and the results are shown below (Table 3).

Table 3. Contact Angle Measurement

	Foil Thickness	Coating	Contact Angle (H2O)
Stencil 1	5 MIL (.127mm)	None	61
Stencil 2	5 MIL (.127mm)	CVD1	107
Stencil 3	5 Mil (.127mm)	CVD2 (PP)	114
Stencil 4	5 MIL (.127mm)	NSG (Ceramic)	114

These contact angles show that the CVD coatings do offer contact angles that are hydrophobic, like that of the ceramic nano-coatings currently available in the SMT stencil market. However, without the Plasma Polishing process, the contact angle is lower than the ceramic nano-coating process. It is assumed the plasma polish process smooths out both the surface of the stencil and the sidewalls of the laser cut apertures prior to the CVD coating process. It is also know that a smoother aperture sidewall releases paste better than rough sidewalls [6]. After the application of the CVD coating on these polished sidewalls the hydro/oleophobic properties should improve paste release.

Another observation is with sprayed on, baked on ceramic nano-coatings, the coating is 2-4 µ thick vs the thickness of a CVD coating of approximately 210 nm or 0.2 µ, just at one-tenth the thickness (Table 4). When the ceramic coating is applied, the coating itself fills the valleys created in the laser cut process and smooths the surface creating improved paste release. The question becomes does the additional process of plasma polishing prior to the CVD process add more variation in thickness and aperture size to the print process. We will discuss this further when looking at solder paste transfer efficiency.

Table 4. Coating Thickness

COATING TYPE	THICKNESS
Self-Assembled Monolayer	0.002-0.004 µ (2-4 nm)
CVD	0.2 µ (210 nm)
NSG (Ceramic)	2-4 µ (2000-4000 nm)

After contact angle was tested, transfer efficiency was calculated for each of the 4 stencils. The uncoated stencil was used as a baseline comparison to the other coatings.

Transfer Efficiency of Solder Paste Deposit

Looking specifically at transfer efficiency or how well the solder paste released from the stencil apertures, the chart below shows the results (Figure 9).

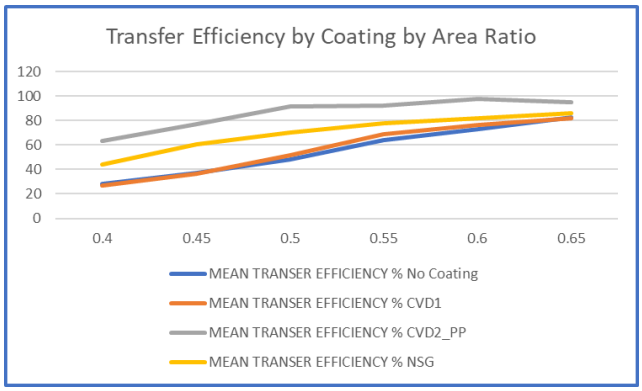

Figure 9. Transfer Efficiency by Coating by Area Ratio

Again, specifically looking at transfer efficiency the CVD2_PP coating performed the best while the NSG ceramic coating performed second best. Note that the CVD1 coating performed only slightly better than the uncoated stencil when looking at this data.

Looking at these results using Tukey Kramer HSD we can determine if the CVD2_PP shows statistically significantly paste release characteristics or not. The results are shown below for an area ratio of 0.45 (Figure 10) and 0.50 (Figure 11).

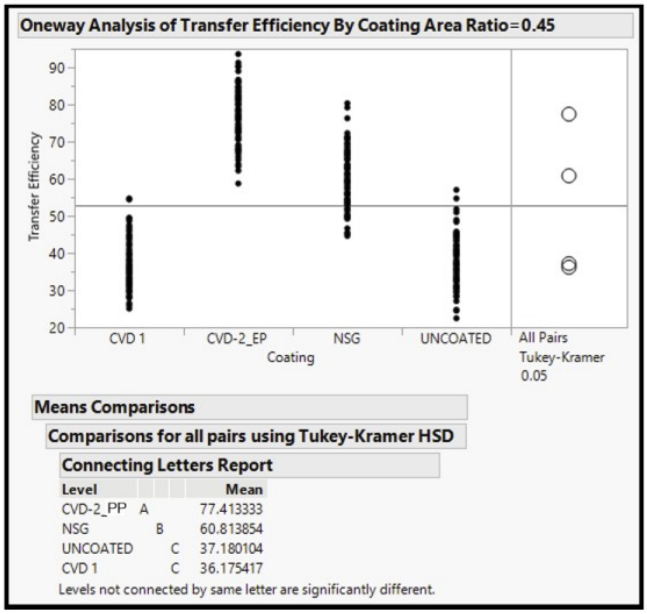

Figure 10. Tukey Kramer HSD, 0.45 Area Ratio

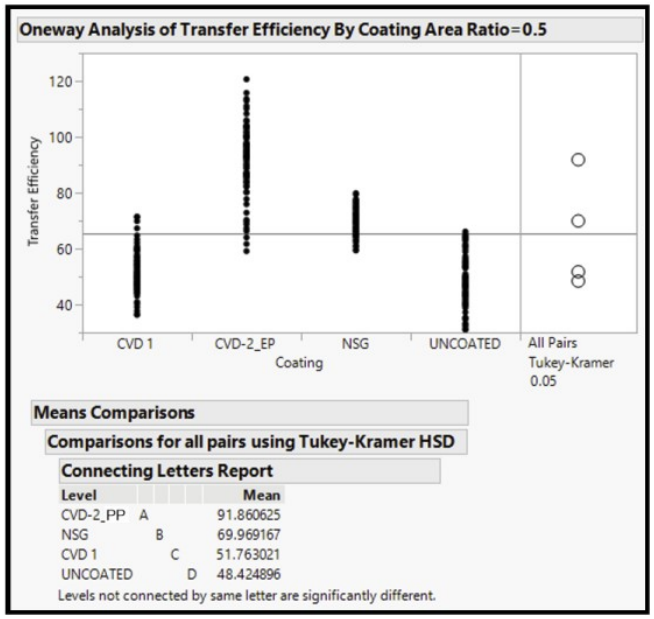

Figure 11. Tukey Kramer HSD, 0.50 Area Ratio

Since the CVD-2PP coating has a different letter assigned than the NSG Ceramic we can say transfer efficiency was statistically better with this coating than the NSG Ceramic coating and both CVD-2PP and NSG Ceramic coating performed better than the CVD1 and Uncoated stencils. For the 0.45 area ratio, the CVD1 coating was not significantly different than an uncoated stencil. When evaluating these coatings strictly based on transfer efficiency, we can show confidently that the CVD-2PP coating produced the highest transfer efficiency.

Coefficient of Variation of Solder Paste Deposit

In addition to transfer efficiency, Coefficient of Variation is critical to maintain an repeatable process window and must be considered when comparing stencil coatings. As product miniaturization continues to push coating development, when printing solder paste using aperture area ratios of less than 0.60, variation or Cv and transfer efficiency must be considered.

Looking at the Coefficient of Variation results below (Table 5) one can see that at area ratios of 0.55 and larger the CVD1, CVD2_PP and NSG Ceramic coatings all produced Cv values less than 10% in the "Good" range. The NSG Ceramic coating was less than 10% at 0.5 for 0.50 area ratio apertures and both the CVD2_PP and NSG Ceramic had Cv values less than 15% for area ratios of 0.45 which is in the "OK" range.

Table 5. Coefficient of Variation (Cv)

	Coefficient of Variation			
Area Ratio	No Coating	CVD1	CVD2_PP	NSG
0.4	20%	25%	16%	17%
0.45	18%	18%	14%	13%
0.5	18%	14%	13%	7%
0.55	14%	9%	8%	6%
0.6	13%	7%	7%	5%
0.65	12%	8%	9%	6%
< 10% Good	10%-15% OK		>15% BAD	

Analyzing both transfer efficiency and Cv for these coatings one can see that although the CVD2_PP coating had the highest transfer efficiency it also had much higher Cv values than the NSG Ceramic Coating (Figure 12) on apertures with area ratios over 0.45. When looking at printing apertures in these very small sizes and low area ratios, reducing variation is just as important as maintaining high print transfer rates [7].

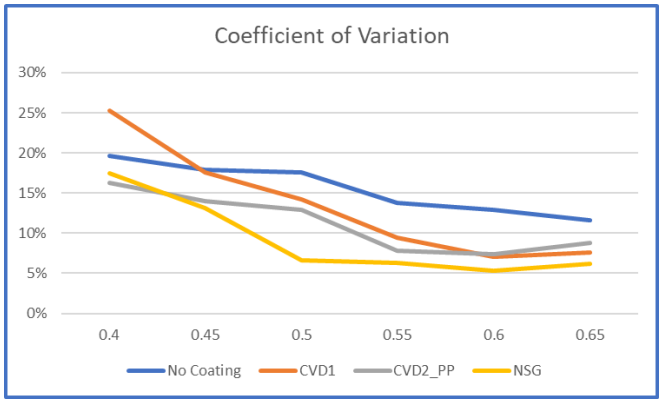

Figure 12. Coefficient of Variation (Cv) Graph

CONCLUSION

Chemical Vapor deposited nano-coatings are a viable coating option for SMT solder paste stencils. When comparing these coatings to current nano-coatings available in North America one can conclude that they do improve transfer efficiency and perform better than self-assembled monolayer nano-coatings currently in use. This can be seen when examining transfer efficiency of solder paste with vapor deposited coating. However, this coating requires a secondary process prior to applying the coating which is a plasma polish process. Without the plasma polish surface preparation process, the coating is not significantly different than an uncoated stencil. In addition, when looking at coefficient of variation in the paste deposits using the CVD coated stencil with plasma polish, we see the Cv values are higher than those of the NSG Ceramic nano-coated stencils. When looking for Cv values less than 10%, NSG Ceramic nano-coated stencils are good to print down to 0.5 area ratios and both the CVD coated stencils with plasma polish and NSG Ceramic coated stencils are good to print down to 0.55 area ratio apertures. Of course, these statements are made using the PCB's, specific solder paste, printer settings and SPI equipment used in this experiment. However, general assumptions can be made that both the NSG Ceramic nano-coating and this new CVD nano-coating with a plasma polish surface treatment prior to application allow area ratios lower than the IPC recommended 0.60 area ratio minimum.

FUTURE WORK

The durability of this coating needs to be examined, both from a hardness and scratch resistance perspective. In addition, chemical resistance needs to be examined to make sure standard chemistry used to clean stencils does not affect the coating. Finally, cost of the coating needs to be evaluated vs other coatings on the market to determine if this is a viable process for coating SMT solder paste stencils.

REFERENCES

1. Chemical Vapor Deposition. (2023, September 16) In Wikipedia. https://en.wikipedia.org/wiki/Chemical_vapor_deposition
2. Klaus Nestlera , Falko Böttger-Hillera , Wolfgang Adamitzkia , Gunther Glowaa , Henning Zeidlera,b* and Andreas Schubertb, ScienceDirect, Plasma Electrolytic Polishing – an Overview of Applied Technologies and Current Challenges to Extend the Polishable Material Range, 2016
3. T. Lentz, G Smith, "Fill the Void IV: Elimination of Inter-Via Voiding", Proceedings of IPC Apex Expo, 2018
4. C. Shea, G. Smith, M. Butler, "Evaluating the Next Generation of Stencil Stepping Technologies", Proceedings of SMTA International, 2018
5. T. Lentz, "Can Nano-Coatings Really Improve Stencil Performance?", Proceedings of SMTA International 2013
6. Solehin Sunar, Maria Binti Abu Baker, Azman Jalar, "Effect of stencil wall aperture on solder paste release via stencil printing", Journal of Physics Conference Series 2169(1):012037, January 2022,
7. C. Shea, G. Smith, R. Welch, "Thin Foil Printing in Today's Miniaturized World: Do Printing Rules Change?" Shea, Smith, Welch, Proceedings of SMTA International, 2021