Root Cause Stencil Design for SMT Component Thermal Lands

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ABSTRACT
Recent studies on stencil design to minimize voiding on quad flat no lead (QFN) thermal lands suggest higher paste volumes create lower voiding percentages. However, volume must be reduced to eliminate the possibility of float during reflow. Thermal land stencil designs on components other than QFN's must also reflect a reduction in printed volume to eliminate float while minimizing void percentages.

The IPC 7525B Stencil Design Guideline [1] recommends a 20% to 50% reduction in the printed area of the thermal/ground plane for leadless chip carrier (LCC) / bottom terminated component (BTC) devices which is a very broad window. This guideline also recommends the window pane design for printing these thermal lands but does not specify the size of the gaps between panes. It also does not specify how close these panes can be printed to the edge of the thermal land without creating shorts to the perimeter leads or creating solder balls on components such as Decawat Packages (D-Pak). This window pane stencil design remains the most used design for the reduction of paste on thermal pads as many other designs such as rounds, diamonds, diagonal pads etc. have not been shown to dramatically impact voiding percentages.

This paper specifically explores the effect of the window pane design on void area percentage after reflow for surface mount technology (SMT) component thermal pads without introducing float to the component. Specific window pane gap sizes, total area printed and distance of the outer pane edges to the copper thermal land edge will be varied to determine guidelines for thermal pad stencil design.

Key words: BTC, LCC, stencil design, window pane, voiding

INTRODUCTION
IPC 7525B 3.2.3.7 [1] states that apertures for termination lands should either have no reduction or a 1.0 mil reduction in width, and no reduction in length. The standard states that corner apertures should be 125% wider than the board land to assist in prevention of rotation of the component during reflow. IPC 7525B also states that apertures for thermal/ground plane should be reduced by 20 - 50% of the area of the thermal plane. Window pane designs are suggested (Figure 1).

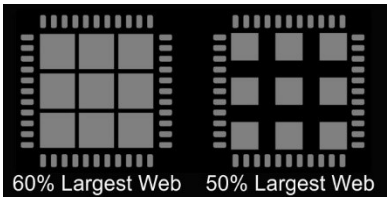

Figure 1. Example of a Window Pane Aperture Design on a Bottom Terminated Component Thermal Pad.

The recommended range of printed solder paste area over thermal pads is very wide (50 - 80%). These areas can be generated using a variety of stencil designs with different web widths, different numbers of solder paste bricks, different perimeter spacings, and so on. What effect do these stencil designs have on wetting / spread of the solder paste? Which stencil design is best for minimizing voiding in the thermal / ground solder joints? The goal of this work is to answer these questions and to optimize the stencil design used for thermal BTC/LCC lands in order to minimize voiding.

EXPERIMENTAL METHODOLOGY
A test board was designed to test a variety of stencil designs on BTC/LCC (Figure 2).

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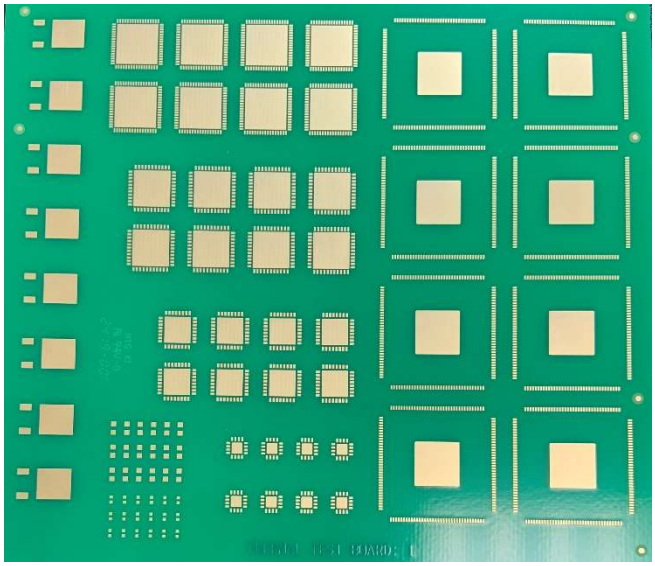

Figure 2. Thermal Pad Test Board.

The thermal pad test board was made of 0.062" thick FR-4 material with a print and etch design, and electroless nickel immersion gold (ENIG) surface finish over 1-ounce copper.

This thermal test board has eight (8) each of a variety of components including: D-Pak, QFP 144 lead, QFN 4 mm, QFN 7 mm, QFN 9 mm, and QFN 10 mm. Many different stencil designs were used for each component on this board. These designs were created to give 50%, 60%, 70%, and 80% area coverage. Within each area of coverage, the following stencil designs were used: largest web, standard web, largest perimeter and most panes possible. There were 16 total individual stencil designs for each component. These were made into two different stencils (Figures 3 and 4).

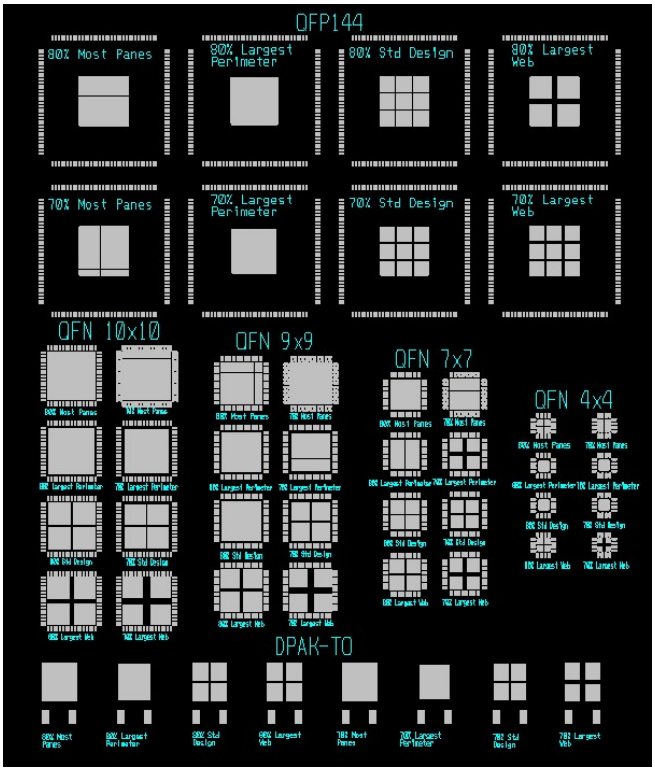

Figure 3. Stencil #1 for the Thermal Pad Test Board Which Includes 70 and 80% Area of Coverage.

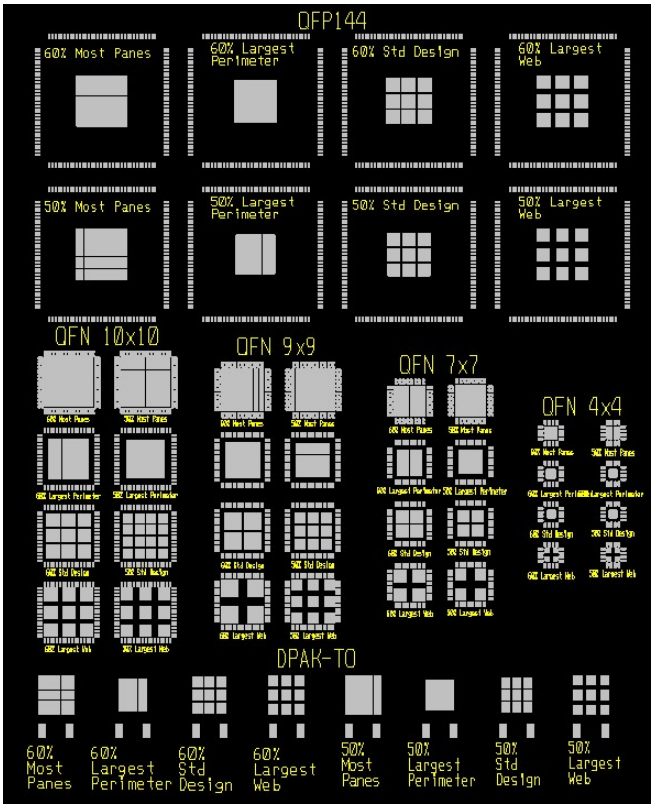

Figure 4. Stencil #2 for the Thermal Pad Test Board Which Includes 50 and 60% Area of Coverage.

The standard design uses the following table to determine the web width while maintaining the overall area of coverage on thermal pads (Table 1).

Table 1. Standard Web Width for QFN/DFN Thermal Pads.

Pad Dimension After Reduction	Web Width
<100 mils	None
101-150 mils	8 mils
150-200 mils	15 mils
>200 mils	20 mils

The details for one of the stencil designs for the QFN 10 mm are shown below (Table 2). The QFN 10 has a thermal pad that is 8.30 mm (327 mils) square.

Table 2. Stencil Design Details for the QFN10 Component.

Paste Area (%)	Desc.	Web Width (mils)	Perim. (mils)	Panes (#)
80	Largest Web	34	1.6	4
80	Standard Web	20	6	4
80	Largest Perimeter	8	10	9
80	Most Panes	8	1.6	20
70	Largest Web	52	1.6	4
70	Standard Web	20	16	4
70	Largest Perimeter	8	18	9
70	Most Panes	8	1.6	49
60	Largest Web	36	1.6	9
60	Standard Web	20	16	9
60	Largest Perimeter	8	29	9
60	Most Panes	8	1.6	100
50	Largest Web	47	1.6	9
50	Standard Web	20	16	16
50	Largest Perimeter	8	38	9
50	Most Panes	8	1.6	144

The stencil design details for the other components were not included in this paper for brevity. The authors would be happy to share the stencil designs if there is interest.

The solder paste used for this work is a commercially available no-clean lead-free solder paste using SAC305 alloy with a Type 4 (20-38 micron) solder powder size. The standard solder paste print parameters used for this testing are shown below (Table 3).

Table 3. Solder Paste Print Parameters.

Printer	Dek Horizon 02
Print Speed	50 mm/sec (varies)
Blade Length	300 mm
Blade Pressure	6.0 Kg
Separation Speed	3.0 mm/sec
Separation Distance	2.0 mm

After printing the solder paste the components were placed and the circuit boards were reflowed. Reflow was done in a 10-zone convection reflow oven using a standard linear ramp to spike type profile in an air atmosphere (Figure 5).

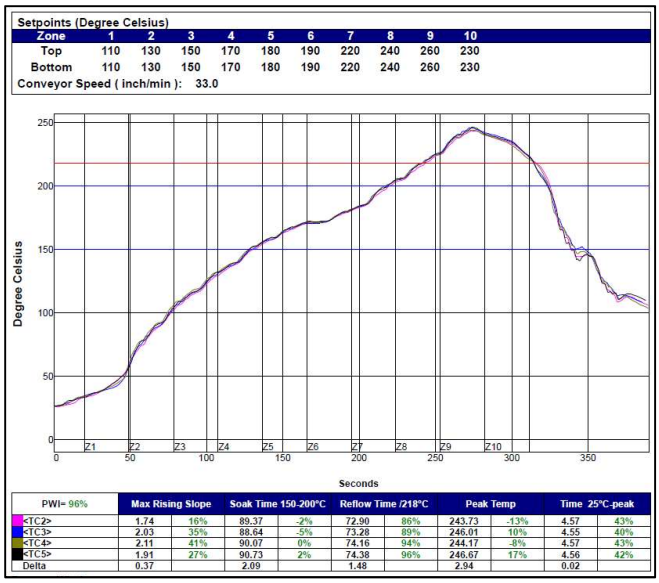

Figure 5. Linear Ramp-to-Spike Reflow Profile.

10 circuit boards were built for each stencil, for a total of 20 circuit boards. A 2-dimensional X-ray was used to measure void area and the size of the largest void on each of the ground/thermal pad solder joints. Essentially 10 void measurements were taken for each variation in stencil design and area of coverage, and there were 80 total variations. The total number of void measurements taken was 800. The solder joints were visually inspected for bridging on the perimeter pads of each component.

Statistical analysis was done to compare the data sets for voiding. The data was displayed in box plot format and Tukey-Kramer honest significant difference (HSD) testing was used to compare the data sets. Tukey-Kramer HSD testing is similar to a Student's T test and is used to determine whether the data sets are significantly different. A 95% confidence level was used in the Tukey-Kramer HSD testing.

RESULTS AND DISCUSSION

D-Paks

Voiding was not able to be measured in solder joints under the D-Pak components due to their density. Instead the solder joints were inspected for wetting and spread to the edges of the pads after reflow. The images below (Figure 6) show wetting and coverage at the thermal pad end of the D-pak components for the standard window pane designs.

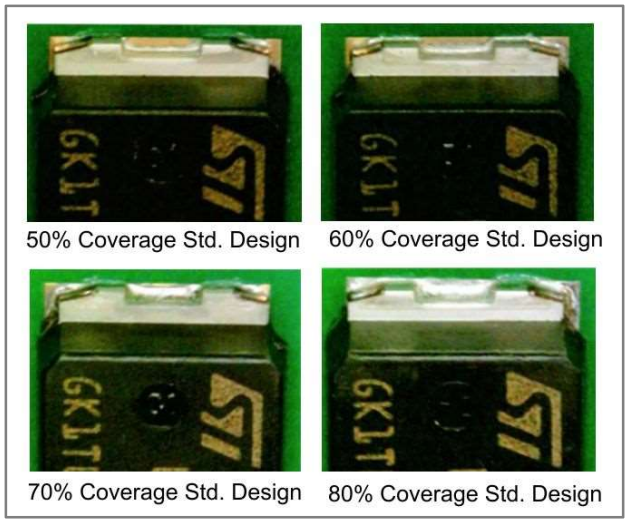

Figure 6. Comparison of D-pak Thermal Pad Coverage after Reflow.

Some of the ENIG is visible on the board pads at the 50 and 60% areas of coverage. The board pads were fully wetted with 70 and 80% areas of coverage.

Voiding Overview

Voiding for the various components used in this work is shown below (Figure 7). This includes all the data from the other variables combined.

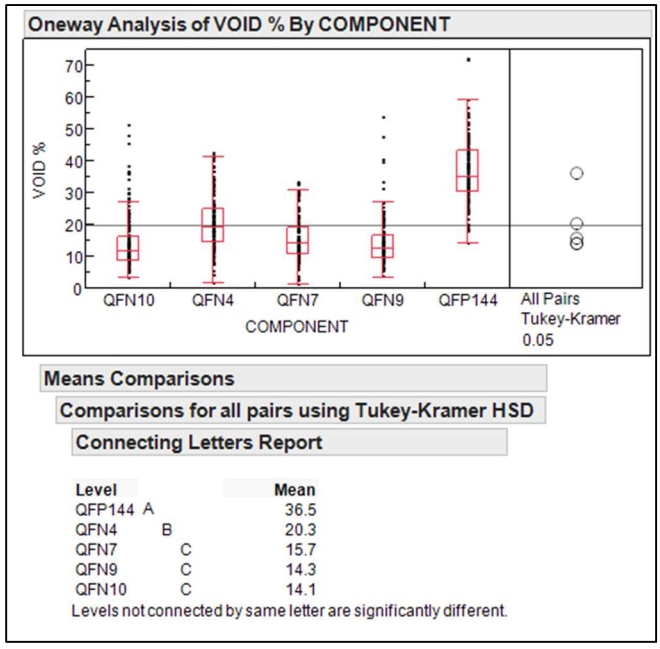

Figure 7. Voiding for Each Component.

The QFP144 gave statistically higher voiding than all of the other components. The QFN4 gave statistically higher voiding than all the other QFNs, which had statistically similar levels of voiding.

Voiding for each area of printed solder paste coverage is shown below (Figure 8).

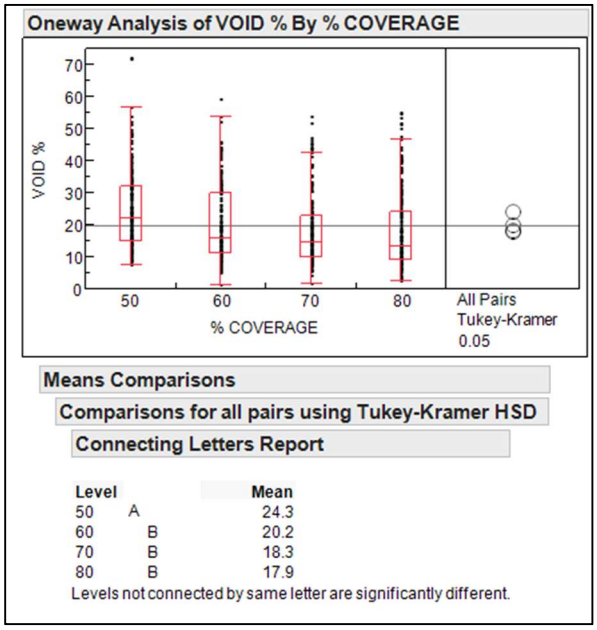

Figure 8. Voiding for Each Area of Coverage.

The 50% area of solder paste coverage gave significantly higher voiding than the other areas of coverage which were statistically similar.

Voiding for each stencil description (design) is shown below (Figure 9).

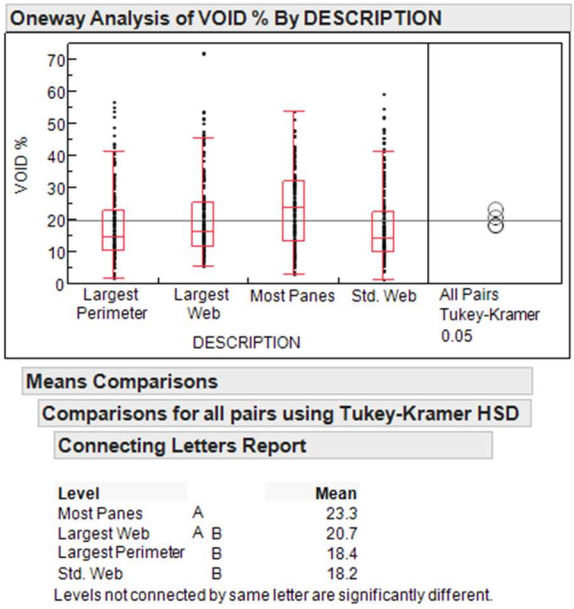

Figure 9. Voiding for Each Stencil Design.

The most panes stencil designs have the highest overall voiding. The largest perimeter and standard web designs gave statistically similar voiding levels which was lower than the most panes design. The largest web design gave statistically similar levels of voiding to the other designs.

Voiding by Coverage

Voiding varied with the area coverage of printed solder paste for each component. All the QFN components showed similar trends in voiding by coverage so only a couple of examples are shown here (Figure 10). These charts include data from all the stencil designs grouped together.

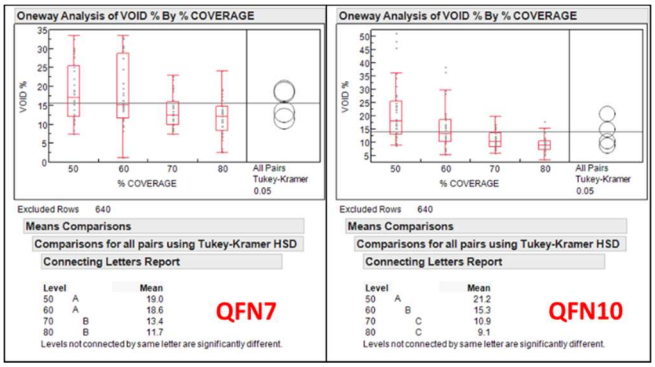

Figure 10. Voiding by Coverage for QFN7 (Left) and QFN10 (Right).

The voiding was highest for the 50 and 60% area coverage with the QFN7 and QFN10 components. The same was generally true for the other QFN components. Voiding decreases with increasing area of coverage, but the difference in voiding for 70 and 80% areas is not statistically significant. Similar results regarding how voiding decreases with increasing solder paste volume have been reported by Nguyen [2] and Herron [3].

The QFP144 component showed equivalent voiding for each area of solder paste coverage (Figure 11).

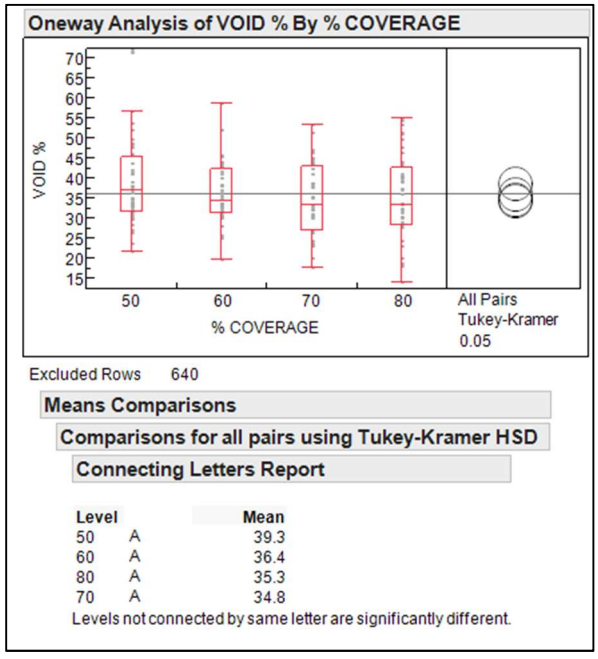

Figure 11. Voiding by Coverage for the QFP144 Component.

The voiding for the QFP144 was high enough overall that it overcame the effects of changing the printed solder paste coverage.

Voiding by Description (Stencil Design)

The voiding varied by description / stencil design. The QFN components showed the same trend in voiding by description regardless of size (Figure 12). These charts include the data from all the areas of coverage grouped together.

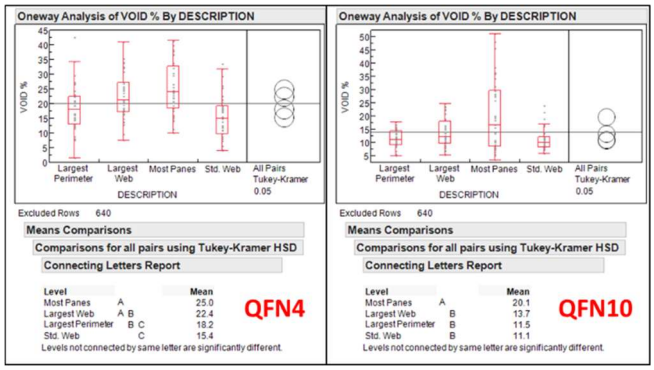

Figure 12. Voiding by Description for QFN4 (Left) and QFN10 (Right).

The most panes design gave the highest voiding and the standard web gave the overall lowest voiding for the QFN components. Below are some representative images of voiding for the QFN10, as they vary by stencil design and area of coverage (Figure 13).

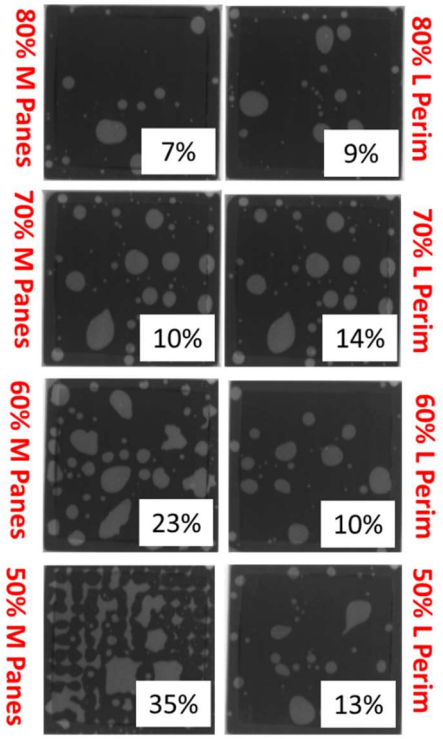

Figure 13. Representative Void Images for the QFN10 Components for the Most Panes and Largest Perimeter Stencil Designs.

Voiding tended to increase for the QFN10s with decreasing area of coverage for the most panes design. The largest perimeter design gave statistically similar levels of voiding for each area of coverage.

The QFP144 did not follow the same voiding trend as the QFN components (Figure 14).

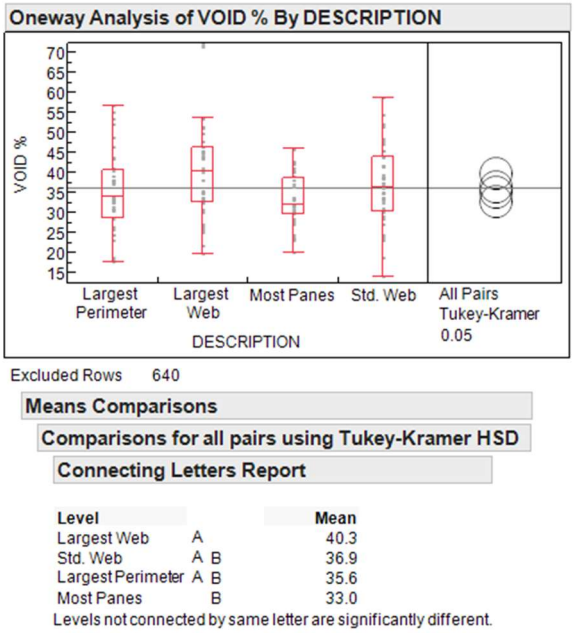

Figure 14. Voiding by Description for the QFP144 Component.

The largest web design gave the highest voiding for the QFP144 while the most panes design gave the lowest overall voiding. Below are some representative images of voiding for the QFP144, as they vary by stencil design and area of coverage (Figure 15).

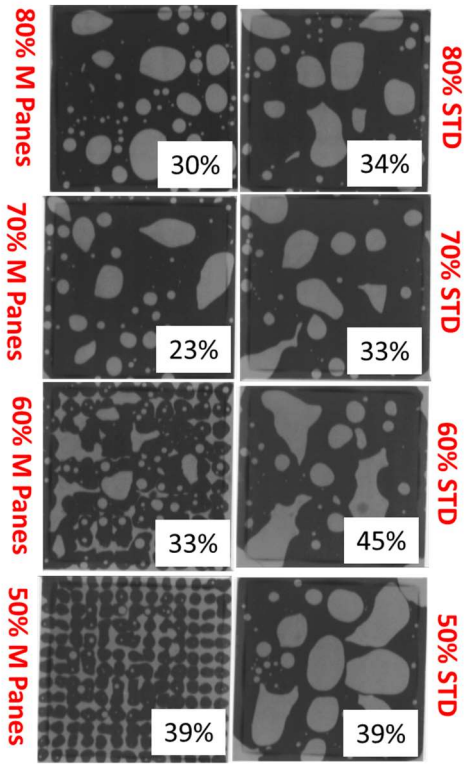

Figure 15. Representative Void Images for the QFP144 Components for the Most Panes and Standard Stencil Designs.

The voiding areas were not statistically different for these different designs, but there are some differences in the appearance of the voids. As the area of coverage decreases in the most panes design, the voids are located along the webs where there are intersections in the gaps between the printed solder paste bricks.

Float/Skew and Bridging

A goal of this work was to count shorts or bridges and record this in the data sets for all components and coverage percentages. The assumption was as percent coverage increased the chances of the component floating and skewing during reflow would increase. For all components, all coverages and all designs, float and skew did not occur during the reflow process. No bridging was seen on any of the components. This was unexpected but may be due to the use of a 4-mil thick stencil. In prior work [4] a 5-mil thick stencil was used with 50-80% area of coverage on QFN ground pads and float was seen at the 80% coverage level. The difference in float and skew between a 4-mil thick and 5-mil thick stencil will be investigated in future work.

CONCLUSIONS

The results for QFN's show that both stencil design and area of coverage affect voiding after reflow. Specifically, the standard window pane and largest perimeter design show the lowest overall voiding results for stencil design. When looking at area of solder paste coverage, the data shows 70% and 80% coverage create the lowest voiding. The combination of these best performing characteristics should

be utilized in the stencil design process to reduce voiding after reflow.

Neither stencil design nor area of solder paste coverage affected QFP void data. It is likely that the overall high levels of voiding for the QFP components overcame the potential effects of changing stencil design and coverage area. There is no conclusive evidence from this work that area coverage and/or stencil design make a difference in reducing voiding on the QFP component used in this study.

Voiding on D-pak components was not able to be measured in this study. However, solder joints were inspected for wetting and spread to the edges of the pads. It was shown that a minimum of 70% coverage is required to create a good solder fillet and achieve complete wetting and spread. All stencil designs show acceptable results at the 70% minimum area coverage.

FUTURE WORK

Reduction of voiding for QFN thermal/ground pads is being investigated as an extension of this work. Stencil designs and reflow profiles will be optimized to minimize voiding on a variety of QFN component sizes. The effects of stencil thickness and overall solder paste volume will be studied with respect to voiding. Modification of the perimeter pad solder volumes will also be studied with respect to voiding on the thermal/ground pads. All of these results will be presented in a future technical paper.

REFERENCES

[1] Stencil Design Task Group (5-21e), "Stencil Design Guidelines", IPC-7525B, October 2011.
[2] J. Nguyen, D. Geiger, M. Kurwa, "Voiding Mitigation for Bottom Terminated Components", Proceedings of SMTA International, 2017.
[3] D. Herron, Y. Liu, N. Lee, "Pad Design and Process for Voiding Control at QFN Assembly", Proceedings of IPC Apex Expo, 2011.
[4] T. Lentz, "Fill the Void III", Proceedings of SMTA International, 2017.